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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/814,483	03/31/2004	Gerald L. Dybsetter	15436.366.1	7758

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EXAMINER	
PATEL, NIMESH G	
ART UNIT	PAPER NUMBER
2111	

MAIL DATE	DELIVERY MODE
10/10/2008	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Advisory Action Before the Filing of an Appeal Brief	**Application No.** 10/814,483	**Applicant(s)** DYBSETTER ET AL.	
	Examiner NIMESH G. PATEL	**Art Unit** 2111	

--The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

THE REPLY FILED 23 September 2008 FAILS TO PLACE THIS APPLICATION IN CONDITION FOR ALLOWANCE.

1. ☒ The reply was filed after a final rejection, but prior to or on the same day as filing a Notice of Appeal. To avoid abandonment of this application, applicant must timely file one of the following replies: (1) an amendment, affidavit, or other evidence, which places the application in condition for allowance; (2) a Notice of Appeal (with appeal fee) in compliance with 37 CFR 41.31; or (3) a Request for Continued Examination (RCE) in compliance with 37 CFR 1.114. The reply must be filed within one of the following time periods:
   a) ☒ The period for reply expires _____months from the mailing date of the final rejection.
   b) ☒ The period for reply expires on: (1) the mailing date of this Advisory Action, or (2) the date set forth in the final rejection, whichever is later. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of the final rejection.

   Examiner Note: If box 1 is checked, check either box (a) or (b). ONLY CHECK BOX (b) WHEN THE FIRST REPLY WAS FILED WITHIN TWO MONTHS OF THE FINAL REJECTION. See MPEP 706.07(f).

Extensions of time may be obtained under 37 CFR 1.136(a). The date on which the petition under 37 CFR 1.136(a) and the appropriate extension fee have been filed is the date for purposes of determining the period of extension and the corresponding amount of the fee. The appropriate extension fee under 37 CFR 1.17(a) is calculated from: (1) the expiration date of the shortened statutory period for reply originally set in the final Office action; or (2) as set forth in (b) above, if checked. Any reply received by the Office later than three months after the mailing date of the final rejection, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

NOTICE OF APPEAL

2. ☐ The Notice of Appeal was filed on _____. A brief in compliance with 37 CFR 41.37 must be filed within two months of the date of filing the Notice of Appeal (37 CFR 41.37(a)), or any extension thereof (37 CFR 41.37(e)), to avoid dismissal of the appeal. Since a Notice of Appeal has been filed, any reply must be filed within the time period set forth in 37 CFR 41.37(a).

AMENDMENTS

3. ☐ The proposed amendment(s) filed after a final rejection, but prior to the date of filing a brief, will not be entered because
   (a) ☐ They raise new issues that would require further consideration and/or search (see NOTE below);
   (b) ☐ They raise the issue of new matter (see NOTE below);
   (c) ☐ They are not deemed to place the application in better form for appeal by materially reducing or simplifying the issues for appeal; and/or
   (d) ☐ They present additional claims without canceling a corresponding number of finally rejected claims.

   NOTE: _____. (See 37 CFR 1.116 and 41.33(a)).
4. ☐ The amendments are not in compliance with 37 CFR 1.121. See attached Notice of Non-Compliant Amendment (PTOL-324).
5. ☒ Applicant's reply has overcome the following rejection(s): 112 rejection of claim 40.
6. ☐ Newly proposed or amended claim(s) _____ would be allowable if submitted in a separate, timely filed amendment canceling the non-allowable claim(s).
7. ☒ For purposes of appeal, the proposed amendment(s): a) ☐ will not be entered, or b) ☒ will be entered and an explanation of how the new or amended claims would be rejected is provided below or appended.
   The status of the claim(s) is (or will be) as follows:
   Claim(s) allowed: _____.
   Claim(s) objected to: _____.
   Claim(s) rejected: *1-40*.
   Claim(s) withdrawn from consideration: _____.

AFFIDAVIT OR OTHER EVIDENCE

8. ☐ The affidavit or other evidence filed after a final action, but before or on the date of filing a Notice of Appeal will not be entered because applicant failed to provide a showing of good and sufficient reasons why the affidavit or other evidence is necessary and was not earlier presented. See 37 CFR 1.116(e).
9. ☐ The affidavit or other evidence filed after the date of filing a Notice of Appeal, but prior to the date of filing a brief, will not be entered because the affidavit or other evidence failed to overcome all rejections under appeal and/or appellant fails to provide a showing a good and sufficient reasons why it is necessary and was not earlier presented. See 37 CFR 41.33(d)(1).
10. ☐ The affidavit or other evidence is entered. An explanation of the status of the claims after entry is below or attached.

REQUEST FOR RECONSIDERATION/OTHER

11. ☒ The request for reconsideration has been considered but does NOT place the application in condition for allowance because: See Continuation Sheet.
12. ☐ Note the attached Information *Disclosure Statement*(s). (PTO/SB/08) Paper No(s). _____
13. ☐ Other: _____.

/Khanh Dang/
Primary Examiner, Art Unit 2111

Continuation of 11. does NOT place the application in condition for allowance because: Applicant's arguments regarding the 112 rejection of claim 40 is persuasive and is withdrawn.

In response to Applicant's arguments regarding Creedon, Examiner explains how Creedon is interpreted. Creedon has a master that sends a preamble that consists of a predetermined number of consectuve bits of the same binary polarity and then sends the rest of the frame. This preamble pattern is used to establish synchroniztion between the components. Creedons's bus is a 2 wire bus, one for data one for clock. The data wire and clock wire use a pull up resistor, causing both wires to be default logic one. If the a logic one wants to be communicated, nothing is done on the data wire, and the clock wire is tied down to zero, and released, causing 1 clock cycle of a logic one. If a logic zero is to be communicated, then the data wire is tied down to zero, and the clock wire is also tied down to zero, causing a clock cycle of logic zero. So, for communicating the preamble, the clock is tied down to zero and released a predetermined number of times(i.e. 32) and nothing is done on data wire. The master is capable of detecting the logic values on the data wire, since it is the only way to know what is being communicated on the data wire. In a 2 wire bus, any component is able to tie down the data wire to logic zero. To communicate in Creedon's system, the master is required to communicate a preamble of 32 consecutive logc ones before the frame starts. While it is communicating this preamble, any component on the bus is able to tie the clock down to zero. If a componet does tie the data wire to zero during this phase, then the requirement of 32 consecutive logic ones is not met ad synchronization is not achieved. It is inherent the master has to monitor the data wire for 32 consecutive logic ones to meet the preamble requirement. One skilled in the art would recognize, in such a bus structure, if it does not monitor the data wire for the correct preamble, errors can occur and synchronization will not be achieved.

As stated in the final rejection, Creedon discloses a system that includes a master component(Figure 1, 10) that is configured to communicate with one or more slave components(Figure 1, 11) over a clock wire(Figure 1, 12) and a data wire(Figure 1, 13), a method for the master component communicating over the data wire while enabling recovery of synchronization between the master component and the one or more slave components, the method comprising the following: determining that an operation is to be performed on a slave component of the one or more slave components(Column 4, Lines 60-61; when required to perform an operation); monitoring the data wire of the two-wire interface upon determining that the operation is to be performed on the slave component; detecting at least the predetermined number of consecutive bits of the same binary polarity have occurred on the data wire during the act of monitoring the data wire(Column 4, Lines 14-18 and 62-67; It is clear that the preamble phase comes after determing an operation is to be performed; voltage level is determined at controlled times; it is inherent the data wire has to be monitored during the preamble phase to ensure synchroniztion, as explained above); and asserting a frame of a two-wire interface on the data wire in response to the act of detecting that the predetermined number of consecutive bits of the same polarity have occurred on the data wire(Figure 4; Column 5, Line 7).

In response to applicant's argument that Creedon sends a start of frame after the preamble phase, regardless of whether any preamble bits are observed r detected, Examiner respectfully disagrees. Nowhere does Creedon say that the start of frame is blindly sent after the preamble phase. As exlained above, it is inherent the master has to monitor the bus for the preamble phase.

In response to Applicant's argument that zero stuffing or bit stuffing is not equivalent to to interpersing a bit with guaranteed minimum frequency, Examiner respectfully disagrees. The reference discloses that if there is control information that is represented by a number of consecutive logic one bits, and if the data is also has the same number of consecutive logic one bits, a zero bit is inserted. Therefore a zero is interperesed in the consecutive ones at a guranteed minimim frequency.